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INTEGRATED CIRCUIT INTERCONNECT

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INTEGRATED CIRCUIT INTERCONNECT

BACKGROUND

An integrated circuit (IC) package is used to electrically couple an IC die to external components and circuitry. An IC package also serves to protect an IC die and to provide a suitable operating environment thereto. These functions may include temperature regulation, impedance matching, and optimization of I/O and power delivery paths. The design of IC package elements may therefore affect the efficiency and/or speed at which an IC die can operate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a top view of an apparatus according to some embodiments.

FIG. 2 is a cross-sectional view of an interconnect according to some embodiments.

FIGS. 3a through 3c are cross-sectional views of interconnects according to some embodiments.

FIG. 4 is a side elevation of an apparatus according to some embodiments.

FIG. 5 is a side elevation of a system according to some embodiments.

DETAILED DESCRIPTION

FIG. 1 is a top view of apparatus 10 according to some embodiments. Apparatus 10 comprises IC package 20 and IC die 30. Apparatus 10 may comprise a microprocessor such as an Intel® PXA800F® cellular processor. Embodiments are not limited to this type of microprocessor or to microprocessors in general.

Package 20 may comprise any ceramic, organic, and/or other suitable material including a physical interface for receiving die 30. According to some embodiments, package 20 is a surface-mountable substrate such as an Organic Land Grid Array substrate

that may be mounted directly onto a motherboard or mounted on a pinned interposer which mates with a socket of a motherboard. Packaging systems other than those mentioned herein may be used in conjunction with some embodiments.

Package 20 includes conductive package pads 25. Conductive package pads 25 may comprise any conductive structure for achieving an electrical connection with an external conductor, including but not limited to a copper pad with nickel and/or gold plating. One or more of conductive package pads 25 may be electrically coupled to microstriplines and/or vias within package 20 that are in turn coupled to external interface elements such as the aforementioned Land Grid Array. Conductive package pads 25 need not be identical to one another, although such an arrangement may simplify their manufacture.

IC die 30 may be fabricated using any suitable substrate material and fabrication technique and may provide any functions. In some embodiments, IC die 30 comprises a microprocessor chip having a silicon substrate. IC die 30 includes conductive die pads 35, which may comprise gold-plated copper contacts. One or more of conductive die pads 35 may be electrically coupled to electrical circuitry that is integrated into die 30.

Interconnects 40 electrically couple the electrical circuitry of IC die 30 to package 20. In some embodiments such as that illustrated in FIG. 1, each of interconnects 40 includes a first end and a second end, with the first end being electrically coupled to one of conductive die pads 35 and with the second end being electrically coupled to one of conductive package pads 25. According to some embodiments, at least one of conductive package pads 25 is electrically coupled to two or more of conductive die pads 35. At least one of conductive die pads 25 is electrically coupled to two or more of conductive package pads 35 according to some embodiments.

At least one of interconnects 40 comprises at least two stranded wires. The at least one interconnect may also include other elements, and is not limited to the at least two stranded wires. The at least two wires are termed "stranded" because they are twisted together or otherwise physically coupled. At least two of the stranded wires in the at least one interconnect 40 are not insulated from each other.

FIG. 2 illustrates a cross-section of one of interconnects 40 according to some embodiments. The illustrated interconnect 40 includes three conductors 41 through 43 of circular cross section. Conductors 41 through 43 are circumscribed by boundary 50. Boundary 50 does not necessarily represent any physical element, but is intended to show an embodiment in which conductors 41 through 43 are disposed within a particular area. In some embodiments, the diameter of boundary 50 is 1 mil. Although boundary 50 is shown as a circular shape, boundary 50 may comprise other shapes according to some embodiments.

Interconnect 40 of FIG. 2 may present less AC skin effect resistance than a single 1 mil wire due to increased surface area. Interconnect 40 may also provide less inductance than the single 1 mil wire due to its multiple current paths. Such effects may be particularly evident at high frequencies.

Conductors 41 through 43 may comprise any conductive material, including but not limited to gold, copper, silver, and conductive polymers. The composition of each of conductors 41 through 43 need not be identical according to some embodiments. Moreover, the shapes of each conductor 41 through 43 may differ in some embodiments. According to some embodiments, conductors 41 through 43 may define a boundary of a shape and/or size that differs from boundary 50.

FIGS 3a through 3c illustrate different configurations of interconnect 40 according to some embodiments. FIG. 3a shows interconnect 40 consisting of two stranded wires, and FIG. 3b shows interconnect 40 consisting of three stranded wires. The two stranded wires of FIG. 3a are of identical shape, the three stranded wires of FIG. 3b are of different shapes, and the three stranded wires of FIG. 3c are of different shapes. Any combination of wire configurations and/or compositions may be used in conjunction with some embodiments. Each different configuration and/or composition may present unique electrical characteristics. A designer may therefore optimize the electrical performance of system 10 by selecting appropriate interconnects according to some embodiments.

As mentioned above, an interconnect according to the invention may comprise two or more stranded wires. Each of these wires may have a first end and a second end. In order to mount such an interconnect as shown in FIG. 1, the first end of each stranded wire may be bonded to a conductive die pad using a first bond. The first bond may be generated using any currently- or hereafter-known system for bonding a single strand of wire to a conductive die pad. In some embodiments, the first ends are bonded to the conductive die pad substantially simultaneously. The second ends of the wires may be bonded to a conductive package pad using a second bond. Again, the second ends may be bonded to the conductive package pad substantially simultaneously.

FIG. 4 shows a side elevation of apparatus 60 according to some embodiments. Apparatus 60 includes package 70 and die 80, which may respectively correspond to package 20 and die 30. Apparatus 60 also includes IC die 90 in a "stacked die" configuration. Die 90 may provide functions that are different from or redundant to the functions provided by die 80.

Die 90 may include conductive die pads (not shown) that are electrically coupled to the circuitry integrated within die 90. The die pads may be electrically coupled to one or more interconnects consisting of two or more stranded wires. A first end of an interconnect may be electrically coupled to a conductive die pad of die 90 and a second end of the interconnect may be electrically coupled to a conductive die pad of die 80. According to some embodiments, a first end of an interconnect may be electrically coupled to a conductive die pad of die 90 and a second end of the interconnect may be electrically coupled to a conductive package pad of package 70.

FIG. 5 illustrates a system according to some embodiments. System 100 includes apparatus 10 of FIG. 1, memory 110 and motherboard 120. System 100 may comprise components of a wireless device platform, or any other suitable platform. Memory 110 may comprise any type of memory for storing data, such as a Single Data Rate Random Access Memory, a Double Data Rate Random Access Memory, or a Programmable Read Only Memory.

Memory 110 and motherboard 120 may be electrically coupled to package 20 of system 100. More particularly, motherboard 120 may comprise a memory bus (not shown) coupled to package 20 and to memory 110. In operation, motherboard 120 may route input/output signals between memory 110 and package 20. The input/output signals may be transmitted between package 20 and die 30 via interconnects 40.

The several embodiments described herein are solely for the purpose of illustration. Some embodiments may include any currently or hereafter-known versions of the elements described herein. Therefore, persons skilled in the art will recognize from this description that other embodiments may be practiced with various modifications and alterations.